

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention

WIRING STRUCTURE FOR INTEGRATED CIRCUIT WITH
REDUCED INTRALEVEL CAPACITANCE

Application Number :

Confirmation Number:

First Named Applicant: Richard Wise

Attorney Docket Number: FIS920030028







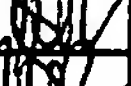

Art Unit:

Examiner:

Search string: (6342722 or 6380106 or 5372969 or 6242336 or 5880026 or 6368939 or 5792706
or 5783481).pn

US Patent Documents

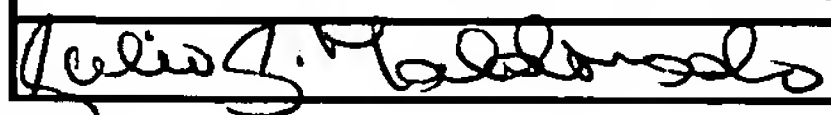
Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	6342722	2002-01-29	Armacost et al.		257	522
	2	6380106	2002-04-30	Lim et al.		438	778
	3	5372969	1994-12-13	Moslehi		438	104
	4	6242336	2001-06-05	Ueda et al.		438	619
	5	5880026	1999-03-09	Xing et al.		438	688
	6	6368939	2002-04-09	Sasaki		438	421
	7	5792706	1998-08-11	Michael et al.		438	622
	8	5783481	1998-07-21	Brennan et al.		438	623

Signature

Examiner Name

Date



09/01/2005